

**CLAIMS**

What is claimed is:

1. A circuit for evaluating duration and/or shape characteristics of an electric pulse induced in an element of an integrated circuit, comprising:

an assembly of elements ( $D_1$  to  $D_n$ ;  $d_1$  to  $d_n$ ), each element being likely to receive an occasional external disturbance generating an electric pulse in the element, and

a measurement circuit ( $B_1$  to  $B_n$ , 1;  $b_1$  to  $b_n$ , 20) connected to the elements to determine said characteristics of an electric pulse generated in one of the elements.

2. The evaluation circuit of claim 1, for an evaluation of the duration of a pulse generated in one of said elements, wherein said elements form a chain of elements ( $D_1$  to  $D_n$ ) in series to propagate a pulse generated in one element through the next elements, the measurement circuit comprising:

storage means ( $B_1$  to  $B_n$ ) for storing at a given time the output levels of the elements; and

a determination means (1; 4) for determining, based on the storage means, the number of elements indicating levels distinct from the idle level.

3. The evaluation device of claim 2, wherein the determination means indicate a duration equal to the number of elements indicating levels distinct from the idle level multiplied by the propagation time through an element.

4. The evaluation circuit of claim 2, wherein the storage means are formed of flip-flops ( $B_1$  to  $B_n$ ) controlled by a same clock signal (CLK), the output of each circuit element ( $D_i$ ) being connected to the data input of a flip-flop ( $B_i$ ), the data output of each flip-flop being connected to the determination means.

5. The evaluation circuit of claim 2, wherein the storage means are formed of flip-flops ( $B_1$  to  $B_n$ ) in series controlled by a same clock signal (CLK) and of several multi-

plexers ( $M_1$  to  $M_n$ ), the output of a flip-flop ( $B_i$ ) being connected to a first input of a multiplexer ( $M_i$ ) having its output connected to the data input of the next flip-flop ( $B_{i+1}$ ), the second inputs of the multiplexers receiving the outputs of the circuit elements ( $D_1$  to  $D_n$ ), the data output of the last flip-flop ( $B_n$ ) being  
5 connected to the determination means.

6. The evaluation device of claim 5, further comprising a detector circuit (5) indicating whether no flip-flop, a single one, or several ones have switched, and wherein the data  
10 output of the last flip-flop ( $B_n$ ) is connected to a counter (4) which counts the number of successive flip-flops, the stored levels of which are distinct from the idle levels, the counter receiving the stored levels in series when the multiplexers ( $M_1$  to  $M_n$ ) are set to have the stored levels pass from one flip-flop to  
15 another at the rate of the clock signal (CLK).

7. The evaluation circuit of claim 6, further comprising a control circuit (6) which:

initially sets the multiplexers ( $M_1$  to  $M_n$ ) in a capture mode by connecting the outputs of the circuit elements ( $D_1$  to  $D_n$ )  
20 to the data inputs of the flip-flops ( $B_1$  to  $B_n$ );

sets the multiplexers in a counting mode to have the stored levels pass from one flip-flop to another when the detector circuit indicates that at least two flip-flops have switched state, and

25 resets the multiplexers in capture mode when the counter indicates the end of the counting.

8. The evaluation circuit of claim 7, wherein the circuit elements ( $D_1$  to  $D_n$ ) are non-inverting circuits and the flip-flops ( $B_1$  to  $B_n$ ) are set to level "0", and wherein the  
30 detector circuit (5) comprises two first OR gates (10, 11), each first OR gate receiving one flip-flop data output out of two, the outputs of the first two OR gates entering a second OR gate (12) and an AND gate (13), the control circuit receiving the outputs of the second OR gate and of the AND gate.

9. The evaluation circuit of claim 7, wherein the circuit elements ( $D_1$  to  $D_n$ ) are inverter circuits and the flip-flops ( $B_1$  to  $B_n$ ) are set, half to level "0" and half to level "1", and the detector circuit (5) comprises a first OR gate receiving the outputs of the flip-flops set to "0", and a first AND gate receiving the outputs of the flip-flops set to "1", the outputs of the first two gates entering a second OR gate (12) and a second AND gate (13), the control circuit receiving the outputs of the second OR gate and of the second AND gate.

10. The circuit of claim 2, wherein the storage means are formed of groups of flip-flops ( $B_1$  to  $B_n$ ) controlled by a same clock signal, each group of flip-flops receiving the outputs of groups of circuit elements, the number of flip-flops being smaller than the number of circuit elements, the data output of each flip-flop being connected to the determination means (20).

11. The circuit of claim 1, for evaluating the shape of a pulse generated in one of said elements, wherein the elements are controlled so that a transistor ( $T_1$  to  $T_n$ ) comprised in each element is non-conductive, the drain or the source of a non-conductive transistor of each element being connected to a common node (N), the measurement circuit measuring the variations of the common node voltage when an external disturbance hits the drain or the source of a transistor connected to the common node.

12. The circuit of claim 11, comprising an amplifier (40) of the common node voltage (N) and several analog flip-flops ( $b_1$  to  $b_n$ ) capable of storing the output voltage level of the amplifier, the flip-flops being controlled by an assembly of clocks ( $Ck_1$  to  $Ck_j$ ) offset with respect to one another.

13. The circuit of claim 11, comprising an analog-to-digital converter (60) of the voltage at the common node (N) providing a digital value of the voltage over  $n$  bits (Bit1, Bit2, Bit3), and several groups of binary flip-flops ( $g_1$  to  $g_j$ ), each group of flip-flops comprising  $n$  flip-flops each capable of storing the value of one of the  $n$  bits, the groups being

controlled by an assembly of clocks (Ck1 to Ckj) offset with respect to one another.

14. The circuit of claim 11, comprising a load circuit (30) capable of setting to order the common node (N) to a given voltage.

15. The circuit of claim 11, wherein each transistor is connected to the common node by a connection, the connections being of same lengths.

16. The circuit of claim 12, wherein the offset clocks (Ck1 to Ckj) are provided by a circuit comprising several chains of delay elements (s1, s2) each receiving a clock signal,

the first delay elements (s1-1, s2-1) of each of the chains introducing different delays (DEL1, DEL2), the outputs of each of the elements of said chains providing said clocks.

17. A method for evaluating duration and/or shape characteristics of an electric pulse induced in an integrated circuit element, comprising the steps of:

forming a circuit comprising a great number of elements, each element being likely to receive an occasional external disturbance generating an electric pulse in the element; and

determining, by means of a measurement device connected to the elements, said characteristics of an electric pulse generated in one of the elements.

18. The method of claim 17 comprising evaluating the duration of a pulse generated in one of said elements, wherein the step of forming a circuit comprises arranging a great number of circuit elements (D1 to Dn) in series in an idle state, each circuit element being connected to propagate to the next circuit element a pulse provided by the preceding circuit element, and wherein the determination step comprises periodically storing in storage means the output level of each circuit element and of determining the number of storage means indicating levels distinct from the idle level.

19. The method of claim 17 comprising evaluating the shape of a pulse generated in one of said elements, wherein the

circuit elements are controlled so that a transistor of each element is non-conductive, the drain or the source of a non-conductive transistor of each element being connected to a common node, and wherein the determination step comprises measuring the  
5 variations of the common node voltage when an external disturbance hits the drain or the source of a transistor connected to the common node.